A 12-bit@40MS/s Gm-C Cascade 3-2 Continuous-Time Sigma-Delta Modulator

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Abstract **– This paper reports the transistor-level design of a 130-nm CMOS continuous-time cascade ΣΔ modulator. The modulator topology, directly synthesized in the continuous-time domain, consists of a third-order stage followed by a second-order stage, both realized using Gm-C integrators and a 4-bit internal quantizer. Dynamic element matching is included to compensate for the non-linearity of the feedback digital-to-analog converters. The estimated power consumption is 70 mW from a 1.2-V supply voltage when is clocked at 240MHz. CADENCE-SPECTRE simulations show 12-bit effective resolution within a 20-MHz signal bandwidth.**†1

I. INTRODUCTION

The in-coming generation of mobile terminals will incorporate WLAN-based connection to the Internet. These systems will require broadband Analog-to-Digital Converters (ADCs) capable of digitizing 20-MHz wideband signals with effective resolutions over 12-bit with the minimum power consumption [1]. Recently, a number of Continuous-Time (CT) Sigma-Delta Modulators (ΣΔMs) have been reported featuring 9-11 bit effective resolution within 15-20 MHz signal bandwidth [2]-[5], which make them very appropriate for broadband telecom systems.

Most of reported CT ΣΔMs Integrated Circuits (ICs) use single-loop topologies because of their potentially lower sensitivity to technology parameter variations – a critical error in CT ΣΔMs [6]. However, as demonstrated in [7], more efficient cascade CT ΣΔMs can be obtained by using a direct synthesis method.

Based on this method, this paper presentes the design and electrical implementation of a cascade 3-2 CT ΣΔM, that includes 4-bit internal quantization and Non-Return-to-Zero (NRZ) Digital-to-Analog-Converter (DAC) in all stages. Dynamic Element Matching (DEM) is used to reduce the effect of mismatch on the linearity of the circuit. The feedforward loop filter is implemented using Gm-C integrators whereas current steering DACs are employed in the feedback loop. The design of these blocks, realized in a 130-nm CMOS technology and using a single 1.2-V supply voltage, is based upon a top-down CAD methodology that combines simulation and statistical optimization at different levels of the system hierarchy. CADENCE-SPECTRE transistor-level simulation results demonstrate that the presented circuit can digitize 20-MHz signals with 12-bit resolution when is clocked at 240MHz.

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II. MODULATOR ARCHITECTURE

The modulator has been designed to fulfil the following requirements: 12-bit within a 20-MHz signal bandwidth. In order to cope with these specifications in an optimal way in terms of power consumption, distribution of the Noise Transfer Function (NTF) zeroes and insensitivity to clock jitter [8], an exhaustive exploration of different CT ΣΔM topologies was done using SIMSIDES [9]. As a result, a fifth-order cascade ΣΔM, shown in Fig.1 †2, was selected. It consists of a 3-2 topology, clocked at f_s = 240MHz , with an internal 4-bit (flash) quantizer and NRZ (current-steering) DAC in all stages in order to minimize the effect of jitter, that according to [8], must be below 3ps rms. An extra feedback branch between the output and the input to the quantizer (DAC_2 in Fig.1) and two D-latches are employed in both stages in order to compensate for the effect of excess loop delay [10].

The modulator has been synthesized in the CT domain as proposed in [7] and implemented using Gm-C integrators. The front-end transconductor uses a different topology than the rest of transconductors in the chain because of the very demanding linearity requirements at the input node.

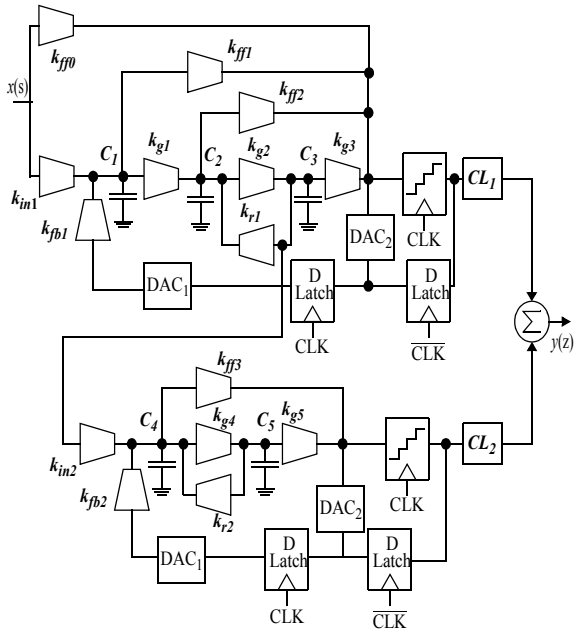

Figure 1. Block diagram of the modulator.

†2. Although the modulator has been implemented using fully-differential circuitry, a single-ended schematic is shown here for the sake of simplicity.

The first stage of the modulator is formed by an integrator and a resonator and the second stage is formed by a resonator. Both resonators have their poles placed at an optimum position, minimizing NTF in the signal bandwidth, B_w [11]. Transconductors can be tuned in order to keep the time constant C/g_m unchanged over C variations. Loop filter coefficients are found through an iterative simulation-based process that – starting from nominal values required to place the NTF zeroes – optimizes the modulator performance in terms of dynamic range and stability within the full-scale range. Table I sums up the outcome of the optimization process – entirely done in the CT domain. This table includes the values of coefficients, k_i (implemented as transconductances) as well as the capacitances, C_i, used in the modulator.

The modulator specifications were mapped onto building-block specifications using statistical optimization for design parameter selection and behavioral simulation for evaluation [9]. The result of this sizing process is summarized in Table II, showing the maximum (minimum) values of the circuit error mechanisms that can be tolerated in order to fulfil the required modulator performance. The data in Table II are the starting point of the electrical design described in next section.

III. CIRCUIT DESIGN

The ΣΔM building blocks, namely, transconductors, current-steering DACs and comparators (used in 4-bit flash quantizers) have been conveniently selected and sized according to the requirements given in Section II[†3]. Design considerations on each of these blocks as well as their transistor-level performance are detailed in this section.

A. Transconductors

One of the main limitations in open-loop Gm-C integrators is their poor linearity. This is specially critical at the input node of the modulator because harmonic distortion caused by the front-end transconductor is directly translated to the digital domain without any attenuation. For this reason, two different transconductors were used in the modulator: one at the front-end and another one for the rest of the loop filter. Fig.2 shows the front-end transconductor, which is based on resistive source degenerated transconductances. Amplifiers are used to improve the linearity of the transconductance. As a triple-well option is available, NMOS transistors are used at the input because body modulation effect can be avoided by connecting the source terminal to the substrate terminal. This circuit was designed considering technology corners and mismatch deviations. Table III shows a summary of the electrical performance.

TABLE I. LOOP FILTER COEFFICIENTS OF THE ΣΔM

$C_u = 3.65$ pF ; $k_u = 190\mu$A/V
$C_1 = C_2 = C_3 = C_u$; $C_4 = C_5 = 2C_u$
$k_{in1} = 852$ μA/V ; $k_{fb1} = 730$ μA/V
$k_{ff0} = 2k_u$; $k_{ff1} = 4k_u$; $k_{ff2} = 2k_u$; $k_{ff3} = 5k_u$
$k_{g1} = k_{g5} = 3k_u$; $k_{g2} = 5k_u$; $k_{g3} = k_u$; $k_{g4} = 7k_u$
$k_{in2} = 5k_u$; $k_{fb2} = 6k_u$
$k_{r1} = k_{r2} = k_u$

†3. In addition to the requirements listed in Table II, the different building blocks are designed such that their thermal noise contribution does not limit the performance of the modulator. This is particularly critical for the front-end transconductor and DAC1.

TABLE II. BUILDING-BLOCK SPECIFICATIONS

Modulator specs: 12-bit @ 20MHz	
Full-scale Reference Voltage	0.5V
Front-End Transconductor	
DC Gain	70 dB
Diff. Input Amplitude	0.3V
Diff. Output Amplitude	0.3V
Third-order non-linearity	−86dB
Loop Filter Transconductors	
DC Gain	50dB
Diff. Input Amplitude	0.3V
Diff. Output Amplitude	0.3V
Third-order non-linearity	−56dB
Flash Quantizers	
Comparator Offset	20mV
Comparator Hysteresis	20mV
Comp. Resolution Time	1ns
Ladder Unit Resistance	220Ω
Current-steering DACs	
Current std. deviation	0.15% LSB
Finite output impedance	12MΩ
Settling Time	500ps

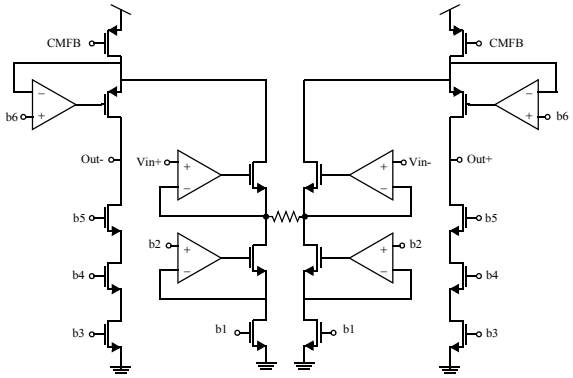

Figure 2. Front-end transconductor schematic.

TABLE III. TRANSISTOR-LEVEL PERFORMANCE OF THE FRONT-END TRANSCONDUCTOR

DC Gain	78.3 dB
Max. Diff. Input Amplitude	0.3V
Max. Diff. Output Amplitude	0.3V
HD3	−89dB
Power consumption	8.8mW

Fig.3 shows the transconductor used for the rest of integrators in the modulator, which is based on a quadratic term cancellation. High-speed operation is achieved by using only feed-forward paths which introduce a high frequency zero that extends the frequency range of operation. This transconductor can be tuned through the bias current, I_{tune}. In order for the tuning to be effective, each transconductance is formed by a parallel connection of unitary transconductors of 100μA/V each. Multiple MonteCarlo simulations have been done during the design process in order to take into account the impact of mismatch on the linearity of this circuit. Table IV shows a summary of the electrical performance of the transconductors showing their main features.

B. Flash quantizers

Embedded quantizers are realized by 4-bit flash ADCs made up of a resistor string for the division of the reference voltage combined with 15 comparators. Non-salicided polysilicon 220-Ω unit resistors were selected according to mismatch and non-linearity requirements.

As far as the comparators is concerned, the circuit shown in Fig.4, based on a regenerative latch including a preamplifying stage, was selected. The role played by the preamplifier is to improve the resolution of the comparator, which can be severely degraded in practice due to dissymmetries between the latch parameters. For that reason, a large number of Monte-Carlo simulations have been done for characterizing the comparator performance after its full sizing. Table V summarizes the comparator features, showing the worst-cases for hysteresis and resolution time, together with the power dissipation.

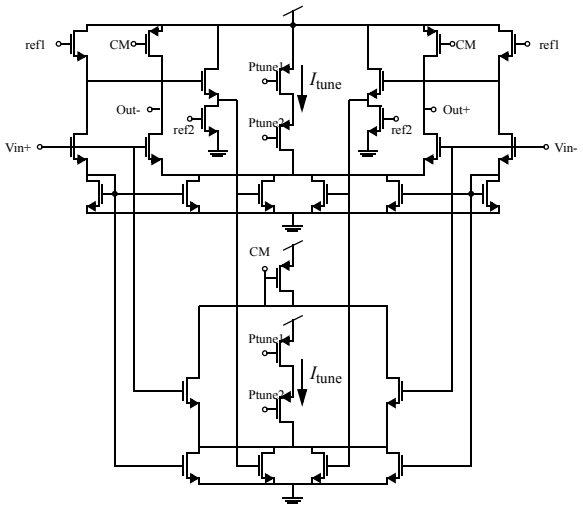

Figure 3. Loop-filter transconductor schematic.

TABLE IV. TRANSISTOR-LEVEL PERFORMANCE OF LOOP-FILTER TRANSCONDUCTORS

DC Gain	52dB
Max. Diff. Input Amplitude	0.3V
Max. Diff. Output Amplitude	0.3V
HD3	–60dB
Power consumption	622μW

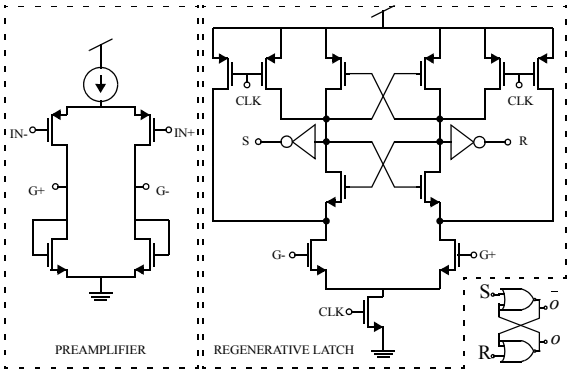

Figure 4. Comparator schematic.

TABLE V. ELECTRICAL PERFORMANCE OF THE COMPARATORS

Parameter	Typical	Worst-case
Offset (mV)	0.7	-3.2
Hysteresis (mV)	12.1	12.7
Resol. time, T_{RLH} (ns)	0.8	0.9
Resol. time, T_{RHL} (ns)	0.75	0.8
Power Cons. (mW)	0.12	

C. Current-steering DACs

Feedback DACs are implemented as current steering DACs because of their potential for high-speed operation and the convenience to interface with Gm-C loop filter [10]. Fig.5(a) shows the block diagram of the circuit. It consists of two 360-μA P-type (Fig.5(b)) gain-boosted current sources and 15 N-type (Fig.5(c)) regulated-cascode current cells which are controlled, through NMOS switches, by a thermometer-code input data (D_i in Fig. 6(a)). The ideal operation of the current cells is affected by random errors (due to device mistmatches), systematic errors (finite output impedance, thermal gradients, edge effects, CMOS technology-related errors) and dynamic limitations. Among the others, there is a strong trade-off

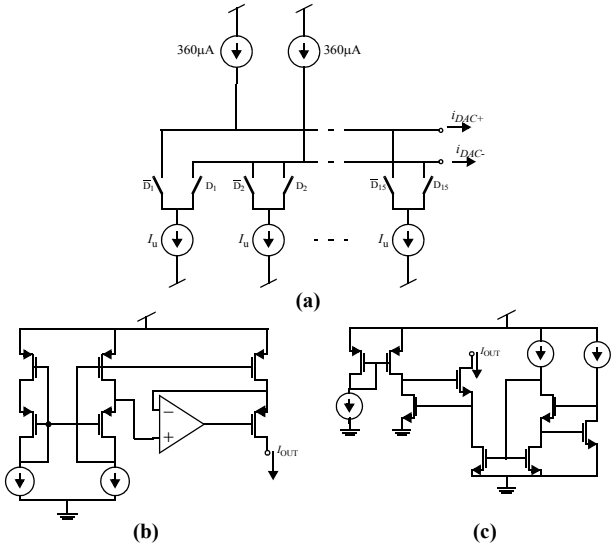

Figure 5. Current-steering DAC. (a) Conceptual block diagram. (b) P-type current cell. (b) N-type current cell.

between required mismatch (0.15% LSB) and settling time (500 ps). In order to relax this trade-off, DEM techniques are used to relax mismatch requirements down to 0.6% LSB, with LSB being $I_u = 48\mu A$, without penalizing the linearity of the modulator. The current cells were sized using FRIDGE [12] and verified by CADENCE-SPECTRE simulations. Table VI sums up the electrical performance[†4], which agrees with specifications given in Table II.

IV. LAYOUT AND TRANSISTOR-LEVEL SIMULATIONS

The modulator has been designed in a 130-nm 1-poly 8-metal logic CMOS process. Metal-insulator-Metal capacitors were used because of their good matching and linearity properties. Fig.6 shows the layout of the chip highlighting the main parts. The layout has been carefully designed to maximize the modulator performance in terms of robustness with respect to switching activity, including separate analog, mixed and digital supplies, guard-rings surrounding each section of the circuit, etc. In addition, centroid layout techniques with unitary transistors have been employed, especially in most critical matched parts of the circuit. The complete modulator occupies an area of 2.33 mm^2 (pads included) and the estimated power dissipation is 70 mW from a single 1.2-V supply voltage.

The modulator has been verified at the transistor-level using CADENCE-SPECTRE. As an illustration, Fig.7 shows the output spectrum for an input sinewave of -10.5-dBV amplitude and 1.348-MHz frequency. The 3rd-order harmonic distortion limits the maximum Signal-to-(Noise+Distortion) Ratio (*SNDR*) to 75.3 dB (12.2 bit) within a 20-MHz band.

TABLE VI. WORST-CASE PERFORMANCE OF CURRENT CELLS

Parameter	P-type cell	N-type cell
Output Impedance	2MΩ	12MΩ
Unitary current	360μA	48μA
Current Std Deviation	0.57%LSB	
Settling Time	--	430ps
Power Cons. (mW)	0.49mW	0.1mW

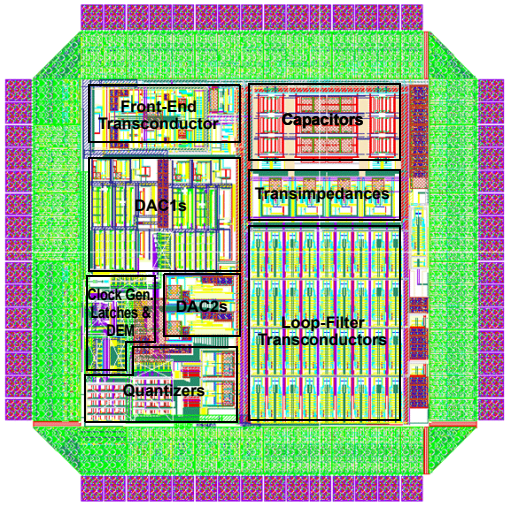

Figure 6. Layout of the modulator.

†4. Note that the P-type current cell is not switched and therefore, the circuit does not need to settle within a given period.

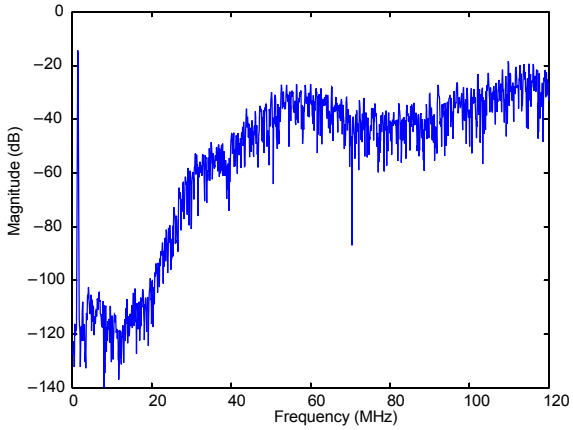

Figure 7. Simulated (SPECTRE) output spectrum of the modulator.

CONCLUSIONS

A 1.2-V, 130-nm CMOS 12-bit@20-MHz cascade 3-2 CT-ΣΔM has been presented. The modulator architecture has been directly synthesized in the continuous-time domain and implemented using Gm-C integrators, 4-bit flash quantizers and NRZ current steering DACs in all stages. The chip has been sent for fabrication and measurements results will be available at the conference. If experimental results agree with CADENCE-SPECTRE simulations, the presented modulator will be at the cutting edge of state-of-the-art on ΣΔMs.

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